REMARKS

I. Formalities

Applicants thank the Examiner for acknowledging the claim for priority under 35 U.S.C. § 119, and receipt of the certified copy of the priority document filed on January 25, 2002.

Applicants note that the Examiner did not indicate whether the Formal Drawings filed on January 25, 2002 are accepted. Applicants respectfully request that the Examiner acknowledge and approve the aforementioned Formal Drawings.

Applicants further note that the Examiner did not initial and return a copy of the PTO Form 1449 submitted with the Information Disclosure Statement filed on January 25, 2002. For the Examiner's convenience, a copy of the PTO Form 1449 is attached. Applicants respectfully request that the Examiner initial and return a copy of the PTO Form 1449.

II. Status of the Application

By the present amendment, claims 1-3 and 10-20 have been amended and claims 21-31 are hereby added to more fully cover various implementations of the invention. Claims 1-31 are all the claims pending in the Application, with claims 1, 3, 12, 14, 21, and 27 being in independent form. Claims 1-20 have been rejected.

The present amendment addresses each point of objection and rejection raised by the Examiner. Favorable reconsideration is respectfully requested.

III. Claim Rejections - 35 U.S.C. § 112

The Examiner has rejected claims 12 and 13 under 35 U.S.C. § 112 as allegedly having insufficient antecedent basis. Applicants have amended claims 12 and 13, as set forth above, to correct the informalities noted by the Examiner. Accordingly, Applicants respectfully request that the Examiner withdraw this rejection.

The Examiner has also rejected claim 14 under 35 U.S.C. § 112, second paragraph, as allegedly being incomplete for omitting essential steps. Applicants have amended claim 14, as set forth above, and submit that claim 14 clearly recites all essential steps. Thus, withdrawal of this rejection is respectfully requested.

IV. Claim Rejections - 35 U.S.C. § 102

The Examiner has rejected claims 1-3, 6-9, 12-14 and 17-20 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,583,527 to Fujisaki *et al.* (hereinafter "Fujisaki"). Applicants respectfully traverse this rejection for *at least* the reasons stated below.

According to the MPEP, "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." MPEP § 2131. Applicants respectfully submit that claims 1-3, 6-9, 12-14 and 17-20 positively recite limitations which are not disclosed (or suggested) by Fujisaki.

A. Independent Claim 1

Independent claim 1 requires (among other things):

> a protection signal output circuit which outputs a first protection signal to said control circuit when a sum of currents supplied from said data drivers to said data electrodes within a time span exceeds a previously set first specified current value...
> wherein said time span is less than one frame.

The grounds of rejection allege that the address current detecting unit 3, together with the comparator 4, as disclosed in Fujisaki, corresponds to a protection signal output circuit, as required by claim 1. Applicants respectfully disagree with the grounds of rejection.

Fujisaki does not disclose or suggest that the address current detecting unit 3, together with the comparator 4, as disclosed therein, outputs a protection signal when a sum of currents within a time span that is less than one frame, exceeds a specified current value, as required by claim 1. In fact, Fujisaki teaches just the opposite—that the address current value to be detected by the address current detecting unit 3 (and subsequently transmitted to the comparator 4) is a value of the address current consumed for each frame (i.e., during a time span equal to one frame). *See* column 9, lines 34-36. Indeed, Fujisaki explicitly teaches that address current values are detected in units of one frame to be displayed on the flat display, or in units of a plurality of frames, and then averaged, for use in controlling the address current flow through the address electrodes. *See* column 10, lines 1-9.

After the address current detecting unit 3 detects current values in units of one frame, moreover, Fujisaki discloses that, comparator 4 then compares the detected address current

values for each frame, or for each plurality of frames, to a reference current value. *See* column 10, lines 40-52. Therefore, since comparator 4 only compares the detected address current values in units of one frame to a reference current value, Fujisaki is incapable of disclosing that the comparator 4 outputs a protection signal when a sum of currents within a time span that is less than one frame, exceeds a specified current value, as required by claim 1.

Thus, the disclosure in Fujisaki is merely cumulative to the display disclosed in Japanese Patent No. 2853537, which is discussed in the present specification on page 14, lines 15-28. That is, since Fujisaki discloses that the detection of current consumption is performed in units of one frame, no protection is performed unless the current consumption in one entire frame exceeds the reference value, even if the current consumption of a particular sub-field, within a single frame, becomes temporarily high.

Therefore, because Fujisaki discloses that the address current detecting unit 3 detects address current values in units of one frame, Fujisaki does not teach, and is incapable of suggesting, that address current detecting unit 3, together with the comparator 4, outputs a first protection signal to a control circuit when a sum of currents supplied from said data drivers to said data electrodes within a time span exceeds a previously set first specified current value, wherein said time span is less than one frame, as required by claim 1.

As a result, Applicants respectfully submit that independent claim 1 is not anticipated by (i.e. is not readable on) Fujisaki for *at least* these reasons. Further, Applicants respectfully submit that the dependent claims 2, 6, and 8 are allowable *at least* by virtue of their dependency

on claim 1. Accordingly, Applicants respectfully request that the Examiner withdraw this rejection.

B. Independent Claim 3

Independent claim 1 requires (among other things):

> wherein said protection signal output circuit outputs a first protection signal when a current from at least one data driver among said data drivers to said data electrode has exceeded a previously set first specified current value; and
>
> wherein said protection signal output circuit judges whether or not a current supplied from at least one data driver among said data drivers to said data electrode has exceeded a previously set second specified current value...

The grounds of rejection allege that the address current detecting unit 3, in conjunction with the comparator 4, corresponds to a protection signal output circuit, as required by claim 3. Applicants respectfully disagree with the grounds of rejection.

Fujisaki does not disclose that address current detecting unit 3, together with the comparator 4, output a first protection signal when a current from at least one data driver has exceeded a previously set first specified current value, and that, in addition, comparator 4 also judges whether or not a current supplied from at least one data driver has exceeded a previously set second specified current value, as required by claim 3.

In contrast to the requirements of claim 3, Fujisaki discloses that the address current detecting unit 3, together with the comparator 4, outputs a control signal to lower the address frequency, after comparing the address current to a single reference current value. *See* column

10, lines 40-52. More particularly, Fujisaki discloses that comparator 4 compares a detected address current value I_a with a single reference current value I_{REF}. *See* column 12, lines 26-27. In fact, Fujisaki provides no suggestion whatsoever that comparator 4 also judges whether or not the address current disclosed therein has exceeded a previously set second specified current value.

Hence, Fujisaki does not disclose (or suggest) a protection signal output circuit which judges whether or not a current supplied from at least one data driver among said data drivers to said data electrode has exceeded a previously set second specified current value, as required by claim 3. Therefore, Applicants respectfully submit that independent claim 3 is not anticipated by (i.e. is not readable on) Fujisaki for *at least* these reasons. Further, Applicants respectfully submit that the dependent claims 7 and 9 are allowable *at least* by virtue of their dependency on claim 3. Thus, Applicants respectfully request that the Examiner withdraw this rejection.

C. Independent Claim 12

Independent claim 12 requires (among other things):

> restraining an operation of data drivers when a sum of currents supplied from said data drivers to data electrodes within a time span exceeds a previously set first specified current value...
> wherein said time span is less than one frame.

In view of the similarity between these requirements and the requirements discussed above with respect to independent claim 1, Applicants respectfully submit that the foregoing arguments as to the patentability of independent claim 1 apply at least by analogy to claim 12.

As such, it is respectfully submitted that claim 12 is patentably distinguishable over Fujisaki *at least* for reasons analogous to those presented above. Further, Applicants submit that the dependent claims 13, 17, and 19 are allowable *at least* by virtue of their dependency on claim 12. Thus, the allowance of these claims is respectfully solicited of the Examiner.

D. Independent Claim 14

Independent claim 14 requires (among other things):

> determining whether or not a current supplied from at least one data driver among data drivers to data electrodes has exceeded a first specified current value;
>
> judging whether or not a current supplied from at least one data driver among data drivers to data electrodes has exceeded a second specified current value; and
>
> restraining the operation of said at least one data driver when the current supplied to said at least one data driver exceeds said second specified current value.

In view of the similarity between these requirements and the requirements discussed above with respect to independent claim 3, Applicants respectfully submit that the foregoing arguments as to the patentability of independent claim 3 apply at least by analogy to claim 14. As such, it is respectfully submitted that claim 14 is patentably distinguishable over Fujisaki *at least* for reasons analogous to those presented above. Further, Applicants submit that the dependent claims 18 and 20 are allowable *at least* by virtue of their dependency on claim 14. Thus, the allowance of these claims is respectfully solicited of the Examiner.

V. Claim Rejections - 35 U.S.C. § 103

The Examiner has rejected claims 4, 5, 15, and 16 under 35 U.S.C. § 103(a) as being unpatentable over Fujisaki in view of JP 11-038930 to Awamoto *et al.* (hereinafter "Awamoto"). The Examiner has also rejected claims 10 and 11 as being unpatentable over Fujisaki in view of U.S. Patent No. 5,956,014 to Kuriyama *et al.* (hereinafter "Kuriyama"). Applicants respectfully traverse these rejections for *at least* the reasons stated below.

A. Independent Claim 1

Applicants respectfully submit that neither Fujisaki, Awamoto, Kuriyama, nor any combination thereof, teaches or suggests all the limitations of independent claim 1. As explained above with respect to claim 1, Fujisaki fails to teach or suggest that the address current detecting unit 3, together with the comparator 4, outputs a protection signal when a sum of currents within a time span that is less than one frame, exceeds a specified current value, as required by claim 1. Furthermore, both Awamoto and Kuriyama also fail to teach or suggest this feature. Consequently, Fujisaki, Awamoto, Kuriyama, and any combination thereof, are incapable of teaching or suggesting the novel limitations of independent claim 1.

Accordingly, claim 1 would not have been obvious from Fujisaki, Awamoto, Kuriyama, and any combination thereof, for *at least* this reason. Further, Applicants submit that the dependent claims 4 and 10 would not have been obvious from Fujisaki, Awamoto, Kuriyama, and any combination thereof, *at least* by virtue of their dependency on claim 1. Thus, Applicants respectfully request that the Examiner withdraw this rejection.

B. Independent Claim 3

Additionally, Applicants submit that neither Fujisaki, Awamoto, Kuriyama, nor any combination thereof, teaches or suggests all the limitations of independent claim 3. As discussed above, with respect to claim 3, Fujisaki fails to teach or suggest that the address current detecting unit 3, together with the comparator 4, output a first protection signal when a current from at least one data driver has exceeded a previously set first specified current value, and that, in addition, comparator 4 judges whether or not a current supplied from at least one data driver has exceeded a previously set second specified current value, as required by claim 3. Moreover, both Awamoto and Kuriyama also fail to disclose or suggest this feature. Consequently, Fujisaki, Awamoto, Kuriyama, and any combination thereof, are incapable of teaching or suggesting the novel limitations of independent claim 3.

Therefore, claim 3 would not have been obvious from Fujisaki, Awamoto, Kuriyama, and any combination thereof, for *at least* this reason. Further, Applicants submit that the dependent claims 5 and 11 would not have been obvious from Fujisaki, Awamoto, Kuriyama, and any combination thereof, *at least* by virtue of their dependency on claim 3. Accordingly, withdrawal of this rejection is respectfully requested.

C. Independent Claim 12

Furthermore, Applicants respectfully submit that neither Fujisaki, Awamoto, Kuriyama, nor any combination thereof, teaches or suggests all the limitations of independent claim 12. In view of the similarity between the recitations of claim 12 and the recitations discussed above with respect to independent claim 1, the foregoing arguments as to the patentability of independent claim 1 apply at least by analogy to claim 12. Hence, it is respectfully submitted

that claim 12 is patentably distinguishable over Fujisaki, Awamoto, Kuriyama, and any combination thereof, *at least* for reasons analogous to those presented above. Further, Applicants submit that the dependent claim 15 is allowable *at least* by virtue of its dependency on claim 12. Thus, the allowance of this claim is respectfully solicited of the Examiner.

D. Independent Claim 14

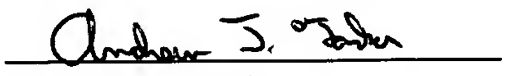
Finally, Applicants respectfully submit that neither Fujisaki, Awamoto, Kuriyama, nor any combination thereof, teaches or suggests all the limitations of independent claim 14. In view of the similarity between the recitations of claim 14 and the recitations discussed above with respect to independent claim 3, the foregoing arguments as to the patentability of independent claim 3 apply at least by analogy to claim 14. Therefore, it is respectfully submitted that claim 14 is patentably distinguishable over Fujisaki, Awamoto, Kuriyama, and any combination thereof, *at least* for reasons analogous to those presented above. Further, Applicants submit that the dependent claim 16 is allowable *at least* by virtue of its dependency on claim 14. Thus, the allowance of this claim is respectfully solicited of the Examiner.

VI. Conclusion

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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Date: September 14, 2005